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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/828,297

04/21/2004

Sung-hee Hwang

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01/31/2006

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EXAMINER

TORRES, JOSEPH D

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 01/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/828,297

Applicant(s)

HWANG ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04/21/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 10/124,366.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/21/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The Office Action cited in the information disclosure statement filed 09/01/2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because it is not in English. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Noda; Chosaku (US 6175686 B1).

35 U.S.C. 102(e) rejection of claim 1.

Noda teaches an error correction code ECC encoder which ECC-encodes main data to generate a plurality of ECC blocks, each of the ECC blocks comprising sectors and each of the sectors having an identifier (Figure 6 in Noda is an ECC Block comprising 16 recording sectors identified by numbers 0 to 15; Figure 7 in Noda is a recording sector comprising 13x182 bytes, that is, an ECC Block is comprised of 16 recording sectors and labeled with identifiers 0-16; col. 12, lines 20-27 and Steps S207 and S208 of Figure 11 in Noda teaches that each channel A and B are error correction encoded to form two ECC blocks one for each channel, each ECC block comprised of 16 recording sectors and labeled with identifiers 0-16, that is, the ECC blocks for channel A and B are generated separately in an identical fashion as would be the ECC block of Figure 6 in the Standard Format, the channel A and B ECC blocks are standard format ECC blocks; Error Correction Processing block S208A generates the channel A standard format ECC block and Error Correction Processing block S208B generates the channel B standard format ECC block; see S208A and S208B in Figure 19 of Noda for details); an interleaver which extracts and arranges the identifiers from ones of the ECC blocks to generate a recording block such that adjacent identifiers are of different ECC blocks (col. 12, lines 39-49 in Noda teach that the channel A and B standard format ECC blocks of Figure 6 are arranged as in Figure 14 to form an extended error correction for which the channel A and B standard format ECC blocks form 2 extended ECC sub-blocks; col. 12, lines 39-49 in Noda teaches that each of the 2 extended ECC sub-

blocks has its own inner and outer parity and, in fact, S208A and S208B in Figure 19 teach that ECC is generate separately and independently for each channel so that each extended ECC sub-block is an independent standard format ECC block; Note: in Figure 14, adjacent identifiers are of different standard format ECC blocks, hence any Channel Synthesis unit for implementing block S211 in Figure 19 of Noda is an interleaver which extracts and arranges the identifiers from ones of the ECC blocks to generate a recording block such that adjacent identifiers are of different ECC blocks); a modulating unit which modulates the generated recording block (S213 in Figure 19 of Noda); and a recording unit which records the modulated recording block (S213 in Figure 19 of Noda).

35 U.S.C. 102(e) rejection of claim 2.

Figure 14 in Noda teaches alternately and equally extracting and arranging the identifiers at predetermined intervals with the ECC-encoded main data included in the sectors corresponding to the arranged identifiers.

35 U.S.C. 102(e) rejection of claim 3.

Figure 14 in Noda teaches interleaving in units of one or more rows.

35 U.S.C. 102(e) rejection of claim 4.

Figure 14 in Noda teaches interleaving in units of at least a part of the sectors.

35 U.S.C. 102(e) rejection of claim 5.

Noda teaches an error correction code encoder to ECC-encode main data to generate first and second ECC blocks, each of the first and second ECC blocks comprising sectors and each of the sectors includes an identifier (Figure 6 in Noda is an ECC Block comprising 16 recording sectors identified by numbers 0 to 15; Figure 7 in Noda is a recording sector comprising 13x182 bytes, that is, an ECC Block is comprised of 16 recording sectors and labeled with identifiers 0-16; col. 12, lines 20-27 and Steps S207 and S208 of Figure 11 in Noda teaches that each channel A and B are error correction encoded to form two ECC blocks one for each channel, each ECC block comprised of 16 recording sectors and labeled with identifiers 0-16, that is, the ECC blocks for channel A and B are generated separately in an identical fashion as would be the ECC block of Figure 6 in the Standard Format, the channel A and B ECC blocks are standard format ECC blocks; Error Correction Processing block S208A generates the channel A standard format ECC block and Error Correction Processing block S208B generates the channel B standard format ECC block; see S208A and S208B in Figure 19 of Noda for details); an interleaver which arranges an identifier included in the first sector of the first ECC block as a first identifier (Sector No. 0 is an identifier included in the first sector of the first channel A standard format ECC block as a first identifier), arranges an identifier included in the first sector of the second ECC block as a second identifier (Sector No. 1 is an identifier included in the first sector of the second channel B standard format ECC block as a second identifier), arranges an identifier included in the second sector of the first ECC block as a third identifier (Sector No. 2 is an identifier included in the second

sector of the first channel A standard format ECC block as a third identifier), arranges an identifier included in the second sector of the second ECC block as a fourth identifier (Sector No. 3 is an identifier included in the second sector of the second channel B standard format ECC block as a fourth identifier), arranging identifiers included in the remaining sectors of the first and second ECC blocks with the same algorithm (see Sector Number 4-31 in Figure 14 of Noda), interleaves ECC-encoded main data in the first sectors of the first and second ECC blocks to sequentially correspond to the first arranged identifier and the second arranged identifier (Figure 14 in Noda teaches that block S211 is an interleaving means for interleaving ECC-encoded main data in the first sectors of the first channel A standard format ECC block and second channel B standard format ECC block to sequentially correspond to the first arranged Sector number identifier 0 and the second arranged Sector number identifier 1), interleaves ECC-encoded main data in the second sectors of the first and second ECC blocks to correspond to the third and fourth arranged identifiers (Figure 14 in Noda teaches that block S211 is an interleaving means for interleaving ECC-encoded main data in the second sectors of the first channel A standard format ECC block and second channel B standard format ECC block to correspond to the first arranged Sector number identifier 2 and the second arranged Sector number identifier 3), and interleaves ECC-encoded main data included in the remaining sectors of the first and second ECC blocks with the same algorithm to generate a recording block (col. 12, lines 39-49 in Noda teach that the channel A and B standard format ECC blocks of Figure 6 are arranged as in Figure 14 to form an extended error correction for which the channel A and B standard format

ECC blocks form 2 extended ECC sub-blocks; col. 12, lines 39-49 in Noda teaches that each of the 2 extended ECC sub-blocks has its own inner and outer parity and, in fact, S208A and S208B in Figure 19 teach that ECC is generate separately and independently for each channel so that each extended ECC sub-block is an independent standard format ECC block; Note: in Figure 14, adjacent identifiers are of different standard format ECC blocks, hence any Channel Synthesis unit for implementing block S211 in Figure 19 of Noda is an interleaver which extracts and arranges the identifiers from ones of the ECC blocks to generate a recording block such that adjacent identifiers are of different ECC blocks); a modulating unit which modulates the generated recording block; and a recording unit which records the modulated recording block (S213 in Figure 19 of Noda); and a recording unit which records the modulated recording block (S213 in Figure 19 of Noda).

35 U.S.C. 102(e) rejection of claim 6.

Figure 14 in Noda teaches alternately and equally extracting and arranging the identifiers at predetermined intervals with the ECC-encoded main data included in the sectors corresponding to the arranged identifiers.

35 U.S.C. 102(e) rejection of claim 7.

Figure 14 in Noda teaches interleaving in units of one or more rows.

35 U.S.C. 102(e) rejection of claim 8.

Figure 14 in Noda teaches interleaving in units of at least a part of the sectors.

35 U.S.C. 102(e) rejection of claim 9.

Noda teaches a reading unit to read data from a recording block of an optical information recording medium, wherein identifiers from ones of error correction code (ECC) blocks are alternately arranged in the recording block, each of the ECC blocks comprising a plurality of sectors having corresponding identifiers (Figure 18 provides a reading unit to read data from a recording block of an optical information recording medium; Figure 6 in Noda is an ECC Block comprising 16 recording sectors identified by numbers 0 to 15; Figure 7 in Noda is a recording sector comprising 13x182 bytes, that is, an ECC Block is comprised of 16 recording sectors and labeled with identifiers 0-16; col. 12, lines 20-27 and Steps S207 and S208 of Figure 11 in Noda teaches that each channel A and B are error correction encoded to form two ECC blocks one for each channel, each ECC block comprised of 16 recording sectors and labeled with identifiers 0-16, that is, the ECC blocks for channel A and B are generated separately in an identical fashion as would be the ECC block of Figure 6 in the Standard Format, the channel A and B ECC blocks are standard format ECC blocks; Error Correction Processing block S208A generates the channel A standard format ECC block and Error Correction Processing block S208B generates the channel B standard format ECC block; see S208A and S208B in Figure 19 of Noda for details); a demodulating unit to demodulate said read data (108 in Figure 18 of Noda); and an ECC decoding unit to decode said de-modulated data (109A and 109B in Figure 18 of Noda).

35 U.S.C. 102(e) rejection of claim 10.

Channel Division circuit 121 in Figure 18 of Noda teaches a de-interleaver to de-interleave said recording block to generate a plurality of reproduced ECC blocks. ECC circuits 109A and 109B in Figure 18 of Noda teach an ECC decoder to decode said demodulated data into main data with an ECC and to output said main data.

35 U.S.C. 102(e) rejection of claim 11.

See Demodulation 108 in Figure 18 of Noda.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-11 provisionally rejected on the ground of nonstatutory double patenting over claims 1-10 and 34-43 of copending Application No. 10/124366. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: both patents are claiming an optical medium for storing identical data structures.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

4. Claims 1-11 provisionally rejected on the ground of nonstatutory double patenting over claims 1-10 and 34-43 of copending Application No. 10/828298. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are

Art Unit: 2133

claiming common subject matter, as follows: both patents are claiming an optical medium for storing identical data structures.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

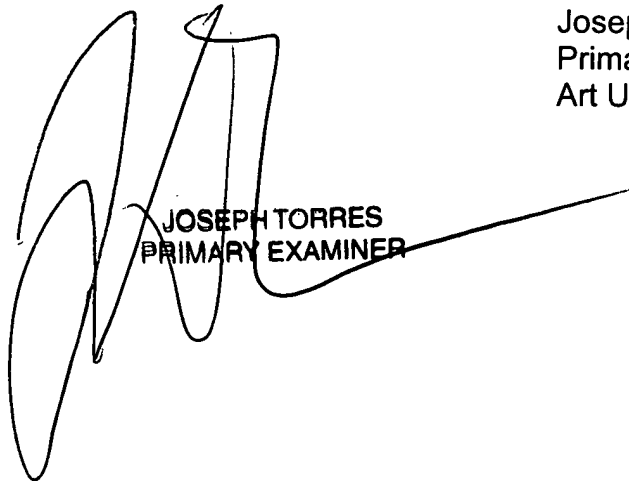
Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2133

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A large, stylized handwritten signature in black ink, consisting of several loops and a long horizontal stroke extending to the right.

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133

JOSEPH TORRES
PRIMARY EXAMINER